IN THE CLAIMS:

Please amend the claims as follows:

1-63. (Canceled).

64. (New) A system, comprising,

a first computer coupled to a second computer;

a second computer coupled to an emulator, wherein the emulator is configured to emulate a design of an integrated circuit having a network interface;

wherein the first computer is configured to send one or more data packets to the second computer at a first speed;

wherein the second computer is configured to:

receive the data packets;

buffer the data packets; and

send data corresponding to the buffered data packets to the emulator at a second speed, wherein the second speed is slower than the first speed; and

wherein the emulator is configured to receive and process the sent data according to the design of the integrated circuit.

65. (New) The system of claim 64, further comprising a third computer coupled to the emulator via a bus;

wherein the emulator is configured to send the processed data to the third computer.

66. (New) The system of claim 64, wherein the second computer is configured to, for each incoming data packet:

examine that data packet;

determine if that data packet is addressed to the emulator; and

if that data packet is addressed to the emulator, buffer that data packet and send data corresponding to the buffered packet to the emulator.

67. (New) The system of claim 64, wherein the emulator is incapable of receiving and processing data sent at the first speed.

68. (New) The system of claim 64, wherein the emulator is implemented, at least in part, using field programmable gate arrays; and

wherein the field programmable gate arrays are operable to be programmed with a hardware model corresponding to the design of the integrated circuit.

69. (New) The system of claim 64, wherein the second computer is further configured to repackage data from the buffered data packets;

wherein the repackaged data is the data the second computer is configured to send to the emulator at the second speed.

70. (New) The system of claim 64, wherein the second computer is further configured to log data corresponding to received data and/or sent data in a log file.

71. (New) The system of claim 65, wherein the third computer is configured to:

receive the processed data; and

examine the received processed data to debug the design of the integrated circuit;

wherein the first computer is coupled to the second computer via a network connection.

72. (New) The system of claim 65, wherein the first computer is configured to generate the one or more packets to be sent to the second computer; and

wherein the generated packets are variable in size.

73. (New) A method, comprising:

a first computer receiving a plurality of data packets at a first speed, wherein the data packets are received over a network connection;

the first computer buffering one or more of the plurality of data packets;

the first computer sending data corresponding to the buffered data packets to an emulator, wherein the emulator is configured to emulate a design of an integrated circuit to be used as a component of a network communication device, and wherein said sending occurs at a speed slower than the first speed;

the emulator receiving and processing the data sent by the first computer, wherein said processing is performed, at least in part, according to the design of the integrated circuit; and

the emulator sending data corresponding to the received and processed data to a second computer.

74. (New) The method of claim 73, wherein the data sent to the second computer is usable to debug the design of the integrated circuit; and

wherein the network connection is an ethernet connection.

75. (New) The method of claim 73, further comprising:

the first computer repackaging data from the buffered data packets;

wherein the repackaged data is the data sent from the first computer to the emulator.

76. (New) The method of claim 73, further comprising the first computer logging contents of one or more of the received data packets in a log file.

77. (New) The method of claim 73, further comprising the first computer logging the sent data in a log file.

78. (New) The method of claim 73, wherein the emulator is configured to emulate a network interface card of the second computer; and

wherein the data is sent to the second computer via a bus coupled to the emulator.

79. (New) The method of claim 73, further comprising the first computer, for each data packet received:

examining that data packet;

determining if that data packet is addressed to the emulator, wherein the emulator is configured to emulate a network interface card of the second computer; and

if that data packet is addressed to the emulator, buffering that data packet and sending data corresponding to the buffered packet to the emulator at the second speed.

80. (New) The method of claim 73, wherein the emulator is implemented, at least in part, using field programmable gate arrays; and

wherein the field programmable gate arrays are operable to be programmed with a hardware model corresponding to the design of the integrated circuit.